XYT--QSFP+_40G SR

RoHS Compliant 40Gb/s QSFP+ SR L1 850nm 100M LC Optical Transceiver

Product Features

●Supports 1.06 to 10.5Gb/s bit rates per Channel
●LC optical connector
●Single +3.3V power supply
●Hot-pluggable QSFP+ MSA form factor
●Up to 100m on OM3 Multimode Fiber (MMF)and 150m on OM4 MMF
●10.7G Electrical Serial Interface
●AC coupling of CML signals
●Low power consumption, <0.8W
●Built in digital diagnostic function
●Operating case temperature range:0℃ to 70℃

Applications

●40GBASE-Ethernet
●Infiniband QDR/DDR/SDR
●40G Datacom connections
●Other optical links

Standards

●Compliant with IEEE 802.3ba
●Compliant with QSFP+ MSA hardware specifications
●Compliant with RoHS

Product Descriptions

Sharetop's XYT--QSFP+_40G SR. The QSFP+ 10G SR L1 optical transceiver is a L1-Channel, Pluggable, Parallel, Fiber-Optic QSFP+ Transceiver for InfiniBand FDR/QDR/DDR/SDR,10G/8G/4G/2G fiber channel, PCIe and SAS Applications. The QSFP full-duplex optical module offers L1 independent transmit and receive channels, 10.7Gbps operation for 100m using OM3 fiber. These modules are designed to operate over multimode fiber systems using 850nmVCSEL laser array.An optical fiber ribbon cable with LC connector can be plugged into the QSFP module receptacle. QSFP+ 10G SR L1 is one kind of parallel transceiver which provides increased port density and total system cost savings.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	Vcc	-0.5	3.6	V	
Storage Temperature	Ts	-40	85	℃	
Relative Humidity	RH	0	85	%	
Damage Threshold, per Lane	DT	3.4		dBm	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Notes
Operating Case Temperature	TC	0	-	+70	℃	
Power Supply Voltage	VCC	3.14	3.3	3.46	V	
Data rate	Dr		10.3	10.7	Gb/s	

Link Distance	Ld			100	m	OM3

Specifications

(tested under recommended operating conditions,unless otherwise noted)

Parameter		Symbol	Unit	Min	Typ	Max	Notes
Voltage Supply Electrical Characteristics							
Supply Current	Tx Section	Icc	A			0.3	
	Rx Section						
Total Dissipation Power		Pw	W			0.8	
Module power supply noise tolerance 10 Hz -10 MHz (peak-to-peak)		PSNR_Mod	mV			66	
Module inrush - initialization time		T_init	ms			500	
Different Signal Electrical Characteristics							
Single Ended Data Input Swing			mV	190		700	
Single Ended Data Output Swing			mV	300		850	
Differential Signal Output Resistance			Ω	90		110	
Differential Signal Input Resistance			Ω	90		110	
3.3V LVTTL Electrical Characteristics							
Input High Voltage		3.3VIH	V	2.0		Vcc+0.3	
Input Low Voltage		3.3VIL	V	-0.3		0.8	
Input Leakage Current		3.3IIN	uA	-10		+10	
Output High Voltage (IOH=100uA)		3.3VOH	V	Vcc-0.2			
Output Low Voltage (IOL=100uA)		3.3VOL	V			0.2	
Minimum Pulse Width of Control Pin Signal		t_CNTL	us	100			
Optical Transmitter Characteristics							
Signaling rate, each lane			GBd	10.3125 ±100 ppm			
Four Lane Wavelength Range		λC	nm	840	850	860	
RMS Spectral Width		Δλrms	nm			0.65	
Average launch power, each lane		Pavg	dBm	-8	+1	0	
Optical modulation amplitude, each lane (OMA)		OMA	dBm	-6	+3	0	
Extinction ratio		ER	dB	3			
Optical return loss tolerance			dB			12	

Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}			{0.25,0.4, 0.45,0.25,0.28,0.4}			
Optical Receiver Characteristics						
Receive Rate for Each Lane		Gbps		10.3125	10.7	
Overload Input Optical Power	Pmax	dBm	+0.5			
Receiver Sensitivity in OMA for Each Lane	SOMA	dBm			-9.5	
LOS Assert		dBm	-30			
LOS Deassert		dBm			-10	

Pin Defintion And Functions

Top side Bottom side

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	10
3	Tx2p	Transmitter Non-Inverted Data Input	10
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	10
6	Tx4p	Transmitter Non-Inverted Data Input	10
7	GND	Ground	1
8	ModSelL	Module Select	3
9	ResetL	Module Reset	4
10	Vcc Rx	+3.3 V Power supply receiver	2
11	SCL	2-wire serial interface clock	5
12	SDA	2-wire serial interface data	5
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	9

15	Rx3n	Receiver Inverted Data Output	9
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	9
18	Rx1n	Receiver Inverted Data Output	9
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	9
22	Rx2p	Receiver	9
22	Rx2p	Receiver Non-Inverted Data Output	1
23	GND	Ground	9
24	Rx4n	Receiver Inverted Data Output	9
25	Rx4p	Receiver Non-Inverted Data Output	1
26	GND	Ground	6
27	ModPrsL	Module Present	7
28	IntL	Interrupt	2
29	Vcc Tx	+3.3 V Power supply transmitter	2
30	Vcc1	+3.3 V Power Supply	8
31	LPMode	Low Power Mode	1
32	GND	Ground	10
33	Tx3p	Transmitter Non-Inverted Data Input	10
34	Tx3n	Transmitter Inverted Data Input	1
35	GND	Ground	10
36	Tx1p	Transmitter Non-Inverted Data Input	10
37	Tx1n	Transmitter Inverted Data Input	1
38	GND	Ground	1

Notes:

1． GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2． Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA. Recommended host board power supply filtering is shown below .

3．The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4．The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

5．Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1.Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology.

6．ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

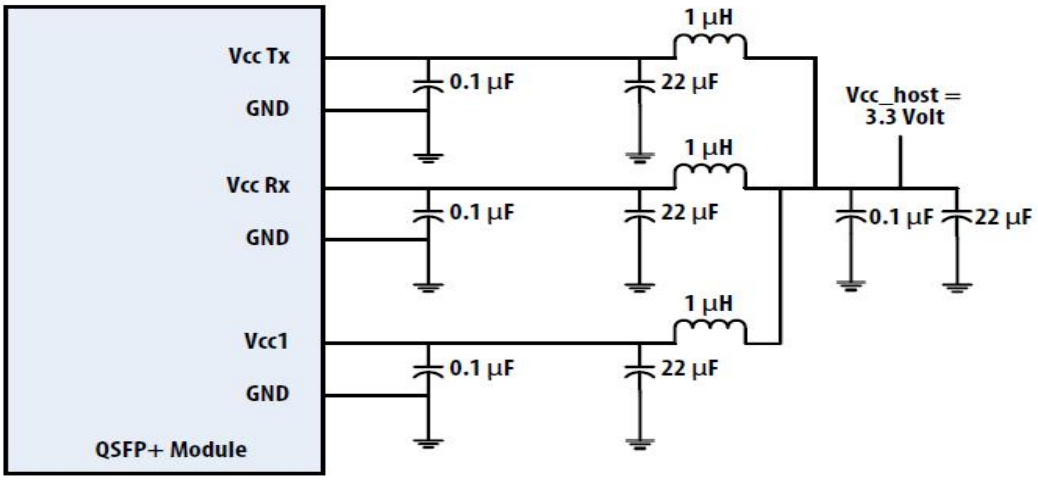
7． IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

8．The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

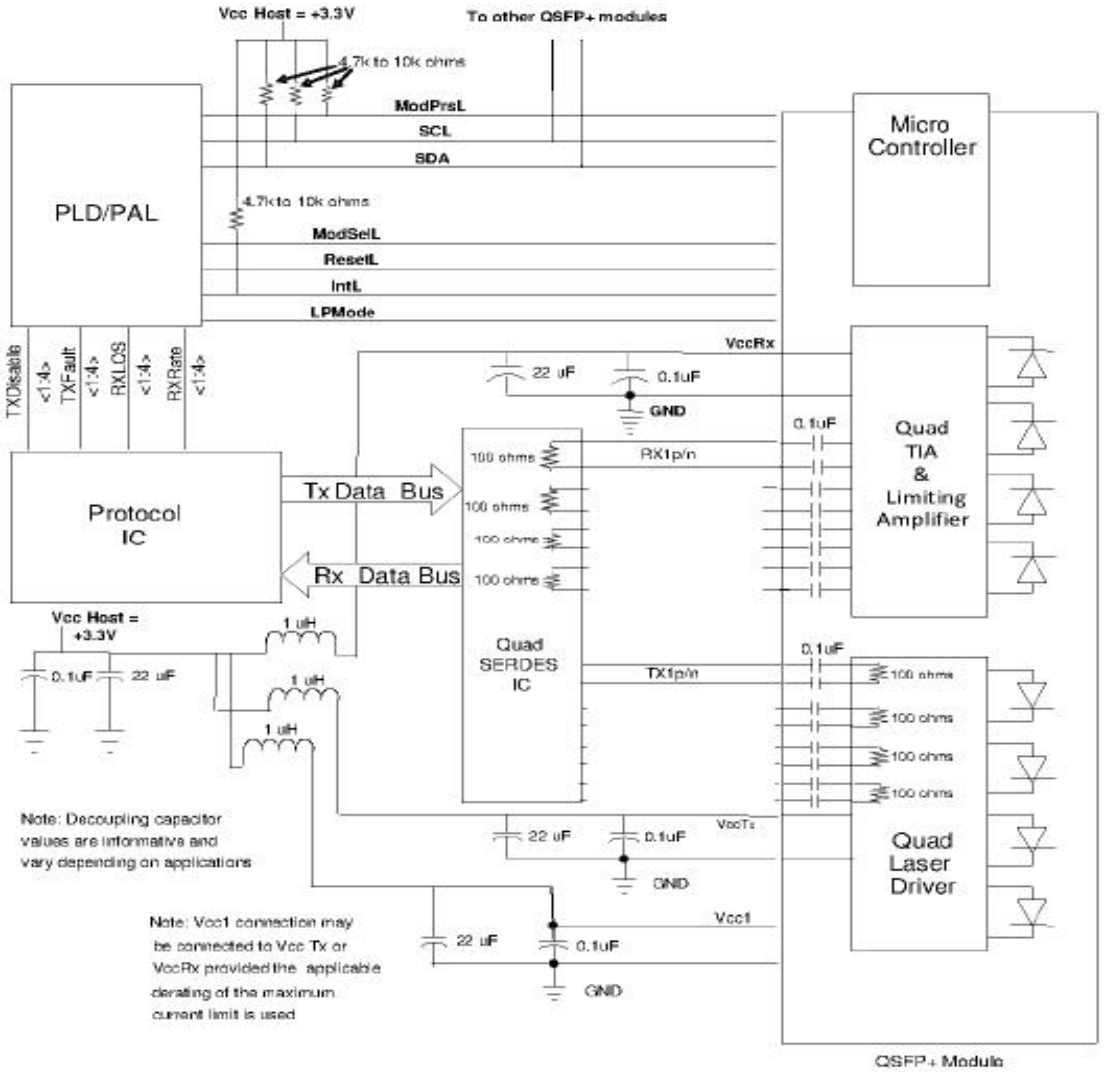
9． Rx(n)(p/n) are module receiver data outputs. The Rx1p and Rx1n are active，the other are NC. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards. Note: Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a host designed for higher speed operation, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential. Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp. In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to SFF-8636.

10．Tx(n)(p/n) are module transmitter data inputs. The Tx1p and Tx1n are active，the other are NC. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards. Due to the possibility of insertion of modules into a host designed for lower speed operation, the damage threshold of the module input shall be at least 1600 mV peak to peak differential. Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended. In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to SFF- 8636.

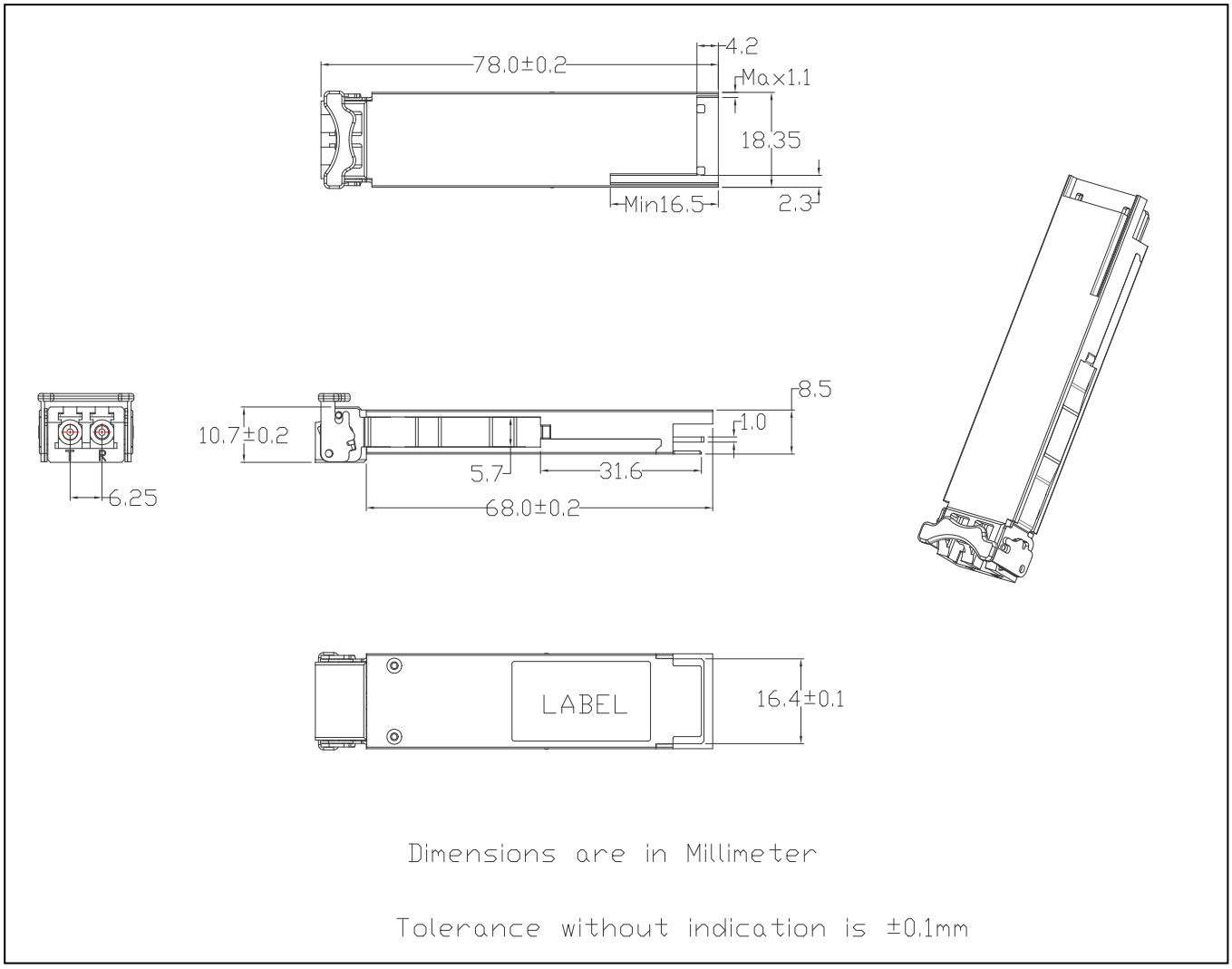
Power Supply Filtering



Recommended Host Board Schematic



Package Dimensions



Ordering Information

Part Number	Description
XYT--QSFP+_40G SR	QSFP+ 10G SR L1 , 100M OM3 Digital Diagnostic Monitor